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(54) **Semiconductor memory cell and memory array with inversion layer.**

(57) A memory cell (10, 50), suitable for electrically erasable programmable read only memories (EEPROMs), which has direct write cell capability is disclosed. The memory cell (10, 50) is fabricated on a substrate (12, 52) and uses an inversion source gate (18, 54) disposed above the substrate (12, 52) to generate a depletion source (IS) therein. The depletion source (IS) defines a channel region in the substrate (12, 52) with an associated drain (14, ID). An electrically isolated floating gate (26, 62) is disposed above the substrate (12, 52) so as to overlap at least a portion of the substrate channel region. Further, a program gate (30, 66) is disposed to overlap a portion of the floating gate (26, 62) and an access gate (34, 70) is also provided aligned at least partially over the substrate channel region such that a dual gate device is defined. An array of such memory cells (10, 50) is also disclosed.

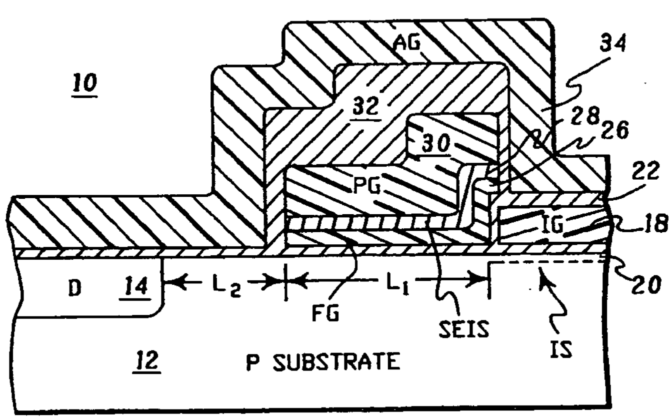

fig. 1b

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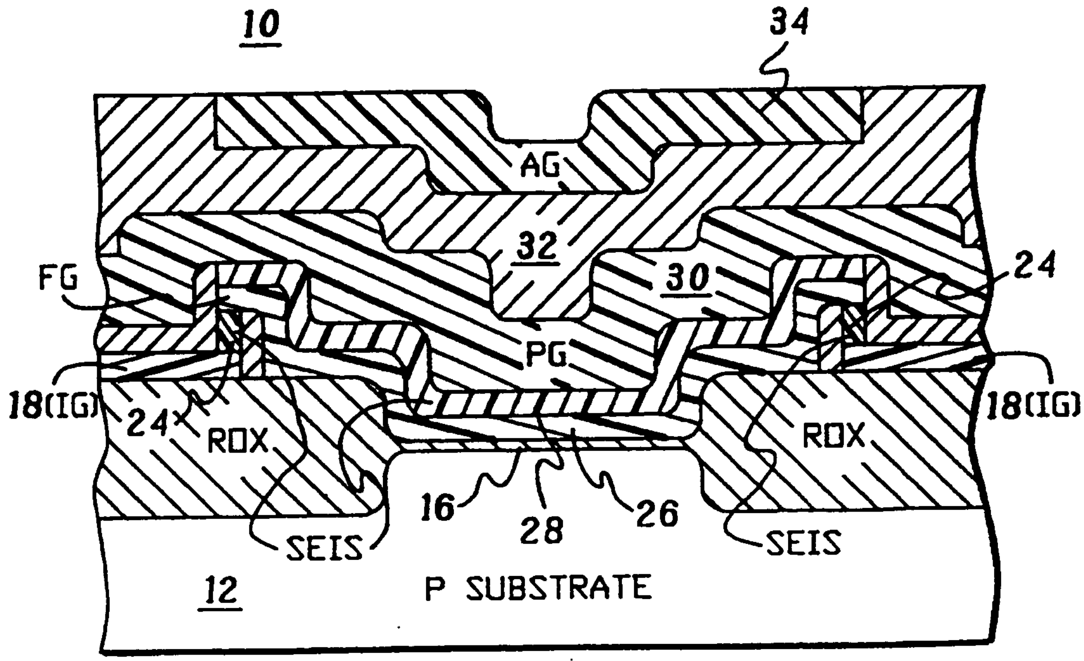
10
34
AG
32
30
FG
24
PG
18(IG)
24
ROX
ROX
18(IG)
16
28
26
SEIS
SEIS
12
P SUBSTRATE

fig. 1c

Background of the Invention

Technical Field

The present invention relates in general to semiconductor memory devices suitable for electrically erasable programmable read only memories (EEPROMs), and more particularly, is directed to MOS floating gate memory cells and memory arrays comprising dense contactless structures with direct write cell capabilities.

Description of the Prior Art

Non-volatile floating gate MOS memories are well known in the industry. In such devices, the conductive state of the transistor memory cell is determined by the voltage of the associated floating gate. Typically, a negatively charged floating gate is representative of a binary one state while an uncharged floating gate is representative of a binary zero state.

More particularly, a conventional electrically programmable read only memory (EPROM) utilizes a floating (unconnected) conductive gate, in a field effect transistor structure, positioned over but insulated from a channel region in a semiconductor substrate, between source and drain regions. A control gate is then provided over the floating gate, but also insulated therefrom. The threshold voltage (V_T) characteristic of the transistor is controlled by the amount of charge that is retained on the floating gate. That is, the minimum amount of voltage (threshold) that must be applied to the control gate before the transistor is turned "on" to permit conduction between its source and drain regions is controlled by the level of charge on the floating gate. A transistor is programmed to one of two states by accelerating electrons from the substrate channel region, through a thin gate dielectric and onto the floating gate.

The memory cell transistor's state is read by placing an operating voltage across its source and drain and on its control gate, and then detecting the level of current flowing between the source and drain as to whether the device is programmed to be "on" or "off" at the control gate voltage selected. A specific, single cell in a two-dimensional array of EPROM cells is addressed for reading by application of a source-drain voltage to the source and drain lines in a column containing the cell being addressed, and application of a control gate voltage to the control gates in a row containing the cell being addressed.

One example of such a memory cell is a triple polysilicon, split channel electrically erasable and programmable read only memory (EEPROM). It is termed a "split channel" device since the floating and control gates extend over adjacent portions of the channel. This results in a transistor structure that operates as two transistors in series, one having a varying threshold in response to the charge level on the floating gate, and another that is unaffected by the floating gate charge but rather which operates in response to the voltage on the control gate as in any normal field effect transistor.

Such a memory cell is termed a "triple polysilicon" cell because it contains three conductive layers of polysilicon material. In addition to the floating and control gates, an erase gate is conventionally included. The erase gate passes through each memory cell transistor closely adjacent to a surface of the floating gate but insulated therefrom by a thin tunnel dielectric. Charge is then removed from the floating gate of the cell to the erase gate, when appropriate voltages are applied to all the transistor elements. An array of EEPROM cells are generally referred to as a "Flash" EEPROM array if an entire array of cells, or a significant group of cells, is erased simultaneously (i.e., in a flash).

Conventionally, to write data into a memory cell, the cell must be first erased and then written. Each of these operations takes approximately ten milliseconds, and each requires, for example, a 20 V supply of voltage. Decoder circuits are used to sustain the needed high voltages at the appropriate cells. These high voltage circuits generally do not scale down in size with the decreasing line widths now attainable with ever improving lithographic techniques. (By comparison, to read a device typically requires three to five volts applied and read cycle times are on the order of hundreds of nanoseconds.) Further, the required step of erasing the floating gate prior to writing data for storage thereon obviously adversely effects the operational speed of a semiconductor array of these type memories.

Summary of the Invention

Briefly summarized, the present invention comprises in one embodiment a memory cell fabricated on a substrate. The cell includes a drain and an inversion source gate. The inversion source gate is dispos d above an upper surface of the substrate such that a depletion sourc is induced in the substrate beneath the gate when a potential is applied thereto. A channel region is defined in the substrate between the drain

and the depletion source. An electrically isolated floating gate, also dispos d above the upper surface of th substrate, is locat d so as to partially overlap the inversion source gat and is electrically isolated therefrom. The floating gate is further align d at least partially over th substrate chann l region. A program gate is also disposed above the upper surface of the substrat and is electrically isolated from the substrate, the inversion source gate and the floating gate. The program gate is located so as to overlap at least a portion of the floating gate. Lastly, an access gate is disposed above the upper surface of the substrate and is electrically isolated from the substrate, inversion source gate, floating gate and program gate. The access gate is directly aligned at least partially over the substrate channel region.

In operation, application of an appropriate potential to the inversion source gate and simultaneous application of a potential to the access gate establishes a cell read cycle to pass charge from the floating gate to the drain. Conversely, application of ground potential to the inversion source gate and simultaneous application of potential to the program gate establishes a cell write cycle to selectively charge the floating gate positively or negatively by respectively grounding or applying voltage to the drain. Additional cell characteristics are also described and claimed herein. For example, in one preferred embodiment, the drain includes an inversion drain gate disposed above the upper surface of the substrate such that a depletion drain is induced in the substrate when a potential is applied thereto.

In another aspect, a memory array fabricated on a substrate is presented. The array includes a plurality of drain lines and a plurality of gate regions. Each gate region is disposed above the substrate adjacent one of the plurality of drain lines and each region includes a floating gate. A plurality of injection source gates are also provided, each of which is disposed above the substrate adjacent to at least one of the plurality of gate regions. Each injection source gate induces a depleted source line in the substrate upon application of an appropriate potential thereto. The depleted source line defines a channel region in the substrate extending to an associated one of the plurality of drain lines. Each defined channel region is at least partially disposed under the associated floating gate. During a read cycle, depleted source lines are established to pass charge through selected ones of the gate regions to their associated drain lines, while during a write cycle depleted source lines are removed to inject charge from selected injection source gates into the floating gates of adjacent gate regions.

The present invention comprises a dense, contactless memory cell having direct write operation such that the conventional block/chip erase operation is eliminated. Further, high voltage decode circuitry for each word line in a memory array is eliminated thereby enhancing memory array density. The contactless design disclosed also serves to minimize cell area. In addition, when in an array structure, blocks of memory cells can be "flash" written, thereby enhancing operational speed. In one embodiment, the invention is implemented in a diffusionless and isolationless design which minimizes generation/recombination centers in the substrate.

Brief Description of the Drawings

These and other objects, advantages and features of the present invention will be more readily understood from the following detailed description of certain preferred embodiments of the present invention, when considered in conjunction with the accompanying drawings in which:

Fig. 1a is a plan view of one embodiment of a memory cell pursuant to the present invention;
Fig. 1b is a cross-sectional view of the memory cell embodiment of Fig. 1a taken along line 1b-1b;
Fig. 1c is a cross-sectional view of the memory cell embodiment of Fig. 1a taken along line 1c-1c;
Fig. 2 is an equivalent capacitive circuit for the memory cell embodiment of Figs. 1a-1c;
Fig. 3 is a schematic diagram of one embodiment of a memory array having multiple memory cells of the embodiment of Figs. 1a-1c;
Fig. 4a is a plan view of an alternate embodiment of a memory cell pursuant to the present invention;
Fig. 4b is a cross-sectional view of the memory cell embodiment of Fig. 4a taken along line 4b-4b;
Fig. 4c is a cross-sectional view of the memory cell embodiment of Fig. 4a taken along line 4c-4c; and
Fig. 5 is a schematic diagram of one embodiment of a memory array having multiple memory cells of the embodiment of Figs. 4a-4c.
Fig. 6 is a table summarizing the voltage bias conditions for a memory cell having the embodiment of Figs. 1a-1c.
Fig. 7 is a table summarizing the voltage bias conditions for a memory cell having th embodiment of Figs. 4a-4c.

Detailed Description of the Invention

One embodiment of a memory cell, g nerally denoted 10, pursuant to the pr sent invention is shown in Figures 1a-1c. Th depicted embodiment comprises an NMOS devic , which is described herein by way of example. A P-type substrate 12 has an N^+-type diffusion region 14 formed therein by typical ion implantation techniques. Substrate 12 could be fabricated of P-type silicon. Those skilled in the art will recognize that memory cell 10 constitutes a floating gate MOSFET device in series with an access MOSFET device. N^+-type region 14 is a diffused bit line which forms the drain (D) of the access device.

Substrate 12 is covered by an oxide layer 16 which is thinly formed in a central region of the cell (see Fig. 1c). A semi-recessed isolation region (ROX) is also grown during this step, using typical techniques. A first polycrystalline silicon layer 18 is then formed on insulating layer 16. In this embodiment, first polycrystalline silicon layer 18 comprises an inversion gate layer (IG) which forms in substrate 12 an inversion source (IS) 20 (Figure 1b) for the floating gate device when a potential is applied thereto, i.e., inversion source 20 is formed in P-type substrate 12 as a depletion source when a potential is applied to gate layer 18. Thus, a channel is formed in the P-type substrate between the diffused drain and the depletion source when one or both of the gates of the split gate structure are activated. The inversion gate (IG) is covered by an oxide layer 22 which is patterned with a layer of single electron injector structure (SEIS) material 24 (Fig. 1c) over selected portions of gate 18. Oxide layer 22 and SEIS material 24 are then covered by a second polycrystalline silicon layer 26 which is etched to form a floating gate (FG). Another SEIS layer 28 is then formed on top of floating gate 26 using conventional techniques. SEIS layer 28 is only formed on the upper surface of floating gate 26; the sides of the floating gate 26 are oxidized to form conventional oxide layers.

A third layer 30 of polycrystalline silicon is deposited to cover the upper surface of SEIS material 28. Layer 30 comprises a program gate (PG) or control gate electrode which preferably overlies all of the floating gate (FG). A further oxide layer 32 is formed to cover program gate layer 30, after which a fourth layer 34 of polycrystalline silicon is deposited. Layer 34 forms the access gate (AG) of the word line device. As shown best in Fig. 1b, cell 10 comprises a split gate device wherein the channel defined between diffused drain 14 and depletion source 20 is controlled for a length L_1 by charge on the floating gate 26 and by the access gate (AG) for a length L_2, which is in series with length L_1. Access gate (AG) is a low voltage decode which is preferably coupled to allow access to an entire word line in a memory array configuration (discussed below).

Note that cell 10 can directly overwrite previously stored data on the floating gate without an intervening erase cycle, which is a significant advantage since the conventional erase operation is time consuming and requires high voltage decode circuitry. Direct overwriting is accomplished pursuant to the present invention by providing the floating gate (FG) with two different areas of electron injection. A first area of electron injection is provided by the program gate (PG) disposed above the floating gate and the second area by the inversion gate (IG) located below and adjacent the periphery of the floating gate. Both areas include a layer of single electron injector structure (SEIS) material which is disposed to facilitate electron injection from the bottom electrode to the top electrode, i.e., from the inversion gate (IG) to the floating gate (FG) or from the floating gate (FG) to the program gate (PG). The size difference between the floating gate (FG) to inversion gate (IG) interface and the program gate (PG) to floating gate (FG) interface effects the capacitance of the respective control gates, which is next discussed in more detail below in connection with the write operation of cell 10.

Initially, the program gate voltage (V_{PG}) and the access gate voltage (V_{AG}) are grounded (0V) and the inversion gate potential (V_{IG}) is set to the chip power supply voltage (V_{DD}) (e.g., 3.3 V). The voltage at the depletion source (V_{IS}) of the floating gate device is charged to V_{DD} - V_T, where V_T is the threshold voltage of the MOS structure. Under these conditions, the floating gate channel L_1 in substrate 12 is depleted of electrons. Programming of the floating gate begins by grounding the inversion gate (IG), thus isolating the floating gate channel, after which the program gate voltage (V_{PG}) is charged, for example, to 20 volts. With the floating gate channel isolated and depleted of mobile charge, the coupling ratio of the floating gate (FG) due to the program gate (PG) is given by equation (1).

$$\chi_1=\frac{C_{FP}}{C_{FP}+C_{FI}+\frac{C_{FN}C_{NS}}{C_{FN}+C_{NS}}} \qquad (1)$$

where $C_{FN} \gg C_{NS}$
Parasitic capacitance, which is presumably small, is neglected in equation 1. The corresponding capacitive n twork for this c ll is shown in Fig. 2, wher nod (N) comprises the surfac of the floating gat chann l and the substrate node comprises the substrate just below the floating gate chann l. The floating gat (FG) is separated from node (N) by thin oxide layer 16 (Fig. 1c) and node (N) is separated from the balance of substrate 12 by the depleted floating gate channel. A practical design value for the coupling ratio $-_1$ of the floating gate due to the program gate (PG) is greater than or equal to .6 with the capacitance between the floating gate and program gate significantly greater than the capacitance between the floating gate and the inversion gate, and with the capacitance of the floating gate to the program gate greater than or equal to the capacitance of the floating gate to node (N), i.e., the surface of the floating gate channel. Hence the initial floating gate voltage is given to be $-_1 V_{PG} \geq V_{PG}/2$.

As a specific example, under the above conditions with the program gate voltage (V_{PG}) set to 20 volts, the floating gate is capacitively coupled to the program gate by the coupling ratio $-_1$ which if assumed to be .6 means that the floating gate voltage (V_{FG}) initially equals 12 V. Since program gate voltage (V_{PG}) equals 20 V, floating gate voltage (V_{FG}) equals 12 V and inversion gate voltage (V_{IG}) equals 0 V, electrons will flow from the inversion gate (IG) towards the floating gate (FG) through SEIS material 24 (Fig. 1b) because of the 12 volt difference therebetween. This electron flow negatively charges the floating gate and drops its potential from 12 volts to approximately 10 volts before the electron flow is discontinued.

In writing a '1', the drain (D) is pre-charged to, and the access gate (AG) is pulsed to, the power supply voltage (V_{DD}). Since the drain and source of the access device are higher than the device threshold voltage (V_T) (floating gate channel being coupled up by the floating gate), the access device is off and the above conditions are unchanged. Electron injection stops when the final floating gate voltage (V_{FG} is approximately equal to $V_{PG}/2$, which accordingly charges the floating gate negatively.

To write a '0', the drain (D) is grounded while the access gate (AG) is pulsed to the power supply voltage (V_{DD}) This turns the access device on discharging the floating gate channel to ground and removing the capacitance between the surface node (N) of the substrate and the substrate, i.e., capacitance (C_{NS}), thereby altering the coupling ratio of the floating gate (FG) due to the program gate (PG). The altered coupling ratio $-_0$ is set forth as equation (2) below.

$$\chi_0 = \frac{C_{FP}}{C_{FP}+C_{FI}+C_{FN}} \qquad (2)$$

With the constraints on the capacitor ratio stated above, a practical design value for coupling ratio $-_0$ is less than or equal to 0.4. Hence the altered initial floating gate voltage is less than $V_{PG}/2$. Assuming the program gate voltage (V_{PG}) equals 20 V, then the initial floating gate voltage (V_{FG}) equals 8 V. Again, since the inversion gate voltage (V_{IG}) is grounded, there is an 8 volt difference between the floating gate (FG) and the inversion gate (IG), while there is a 12 volt difference between the floating gate (FG) and the program gate (PG). Under this biased condition, electrons are injected from the floating gate (FG) onto the program gate (PG), thus charging the floating gate (FG) positive. Again, electron injection stops when the final floating gate voltage (V_{FG}) (i.e., approximately $V_{PG}/2$) is reached.

In practice, equilibrium is typically reached at other than exactly one half V_{PG}. This is because the floating gate (FG) and the program gate (PG) interface over a large surface area while the floating gate (FG) and the inversion gate (IG) interface over a small area. In evaluating the resistive network, there is a greater voltage drop between the floating gate and the inversion gate than there is between the floating gate and the program gate so in both cases there will be a slightly higher positive charge than ideally anticipated. For example, instead of reaching equilibrium at exactly 10 volts, it may be reached at 10.8 - 11 volts. Obviously, surface areas can be adjusted to select an optimum point for design purposes. The particular voltage at which charge transfer stops depends upon the geometry used.

Note that the structure described advantageously requires only the initial setup of conditions for the writing of a zero or a one (i.e., positive or negative charging of the floating gate). There is no need to wait for the cell to reach equilibrium before proceeding to the next memory cell. Further, when assembled in a memory array as discussed below, a block of cells can be accessed sequentially one word line at a time with the program gate (PG) at voltage V_{PG} (e.g., 20 volts) throughout all the access cycles. In this way, conventional high voltage decode circuitry for the writing of each word line is eliminated.

To accomplish a read operation, th program gate (PG) is ground d, th inversion gate (IG) is tied to the power supply voltage (V_{DD}) and the access gat (AG) is pulsed to the power supply voltage (V_{DD}). In cas of a stor d '1', th floating gate is negatively charged so no current path exists b tween the drain (D) and the inversion source (IS), whil in th case of a stored '0', the floating gate is positively charged and a current path exists between the drain (D) and the inversion source (IS). The presence or absence of a current path is sensed at the drain (D).

Fig. 6 summarizes the voltage bias conditions for both read and write operations for a memory cell (or memory array) pursuant to the present invention having the embodiment of Figures 1a-1c.

A sample schematic of a memory array pursuant to the present invention is depicted in Fig. 3. The circuit shown comprises a four by four array of memory cells 10, each of which includes an access MOSFET device 40 and a floating gate MOSFET device 42. The array is divided into an even number of interlaced blocks (e.g., BLK 1, BLK 2) which need not be physically adjoining. The access gates (AG) of each word line (i.e., horizontal row) are all interconnected. Thus, in this embodiment one half of the memory cells in a single row will be accessed each time a particular row is selected, i.e., assuming only block BLK 1 or BLK 2 has been selected. A particular block is selected by applying 20 volts to the corresponding program gates (PG), which as noted above are connected together for a given block. The program gate voltage (V_{PG}) of a selected block stays at 20 volts until an entire selected block is accessed during a write cycle. With a memory array as set forth herein, the cells within an entire block can be "flash" written. As shown, adjacent memory cells can share drain lines and source lines resulting in a more compact array.

An alternate embodiment of the memory cell device and array depicted in Figs. 1a-3, is shown in Figs. 4a-5. The basic structure and concept of operation in both cells is identical except as otherwise noted.

In writing a logical '1' both memory cell embodiments rely on depletion capacitance in a floating gate channel to obtain a high coupling ratio from the program gate (PG) to the floating gate (FG). As memory cell size shrinks with increasingly fine lithography, floating gate capacitance (C_{NS}) decreases. As such, generation current in the depletion capacitor becomes the governing factor in retaining the depletion capacitor. The depletion capacitor must be maintained throughout the write operation, which can be as long as a millisecond. Dislocations and other defects in the depletion region are generation/recombination centers which will enhance generation current. Trench isolations and diffusions are two main sources of such defects in the silicon. To minimize generation/recombination centers, this embodiment of the invention comprises a penta-polysilicon cell 50 wherein trench isolation and diffusion of the initially described memory cell are eliminated (see Figs. 4a-4c). More particularly, a thin oxide layer 51 covers a P-type substrate 52. Layer 51 is particularly thin at a central region of the cell 50 where the floating gate stack is to be located. A first polycrystalline silicon layer is formed on insulating layer 51 and patterned for an inversion source gate (SG) 54 and an inversion drain gate 56 (DG). Gates 54 & 56 respectively define an inversion source layer (IS) and an inversion drain layer (ID) in P-type substrate 52 when appropriate potentials are applied thereto.

The inversion gates are covered by additional oxide and a second polycrystalline silicon layer is deposited and patterned to pass over at least partially the first polycrystalline silicon layer definitive of the inversion source gate (SG) and the inversion drain gate (DG). The second polycrystalline silicon layer is itself patterned as an isolation plate (IP) 57 and is disposed such that when maintained at ground potential cell 50 is isolated from adjacent cells (not shown) in an array. The isolation plate (IP) 57 is covered by an oxide layer 58 which is patterned with a layer of single electron injector structure (SEIS) material 60 (Figure 4c) over selected portions of the isolation plate 56.

Oxide layer 58 and SEIS material 60 are then covered by a third polycrystalline silicon layer 62 which is etched to form a floating gate (FG). Another SEIS layer 64 is formed on top of floating gate 62 using conventional techniques. SEIS layer 64 is only formed on the upper surface of floating gate 62; the sides of the floating gate (FG) are oxidized to form conventional oxide layers. A fourth layer 66 of relatively thick polycrystalline silicon is deposited on the upper surface of SEIS 64. Layer 66 comprises a program gate (PG) electrode which preferably overlies all of the floating gate (FG). A further oxide layer 68 is formed to cover program gate layer 66, after which a fifth layer 70 of polycrystalline silicon is deposited. Layer 70 forms the access gate (AG) of the word line device. As with the previous embodiment, the memory cell of Figures 4a-4c comprises a split gate device where the channel defined between the depletion drain and the depletion source is controlled for a central length L'_1 by charge on the floating gate 62 and for lengths L'_2 by the access gate 70, which as noted in Fig. 4b is directly aligned over the substrate on both sides of the floating gate. As with the prior embodiment, length L'_1 is in series with lengths L'_2 such that a split gate device is established.

Operationally, cell 50 is analogous to cell 10, the major exception being that th diffused drain has been eliminated in cell 50 and replaced by an inversion drain gate (DG) which, when appropriate potential is

applied, establishes a depletion drain (ID) in th substrate. Additionally, the trench isolation r gions (ROX) of the previous embodiment are omitt d from c ll 50. These oxide regions are replaced by an appropriately patterned isolation plat 57, which in this mbodiment is maintained at ground to isolate c ll 50 from adjacent cells in a memory array. Thus, the two main sources of dislocations and other def cts in the substrate of the cell 10 embodiment (Figures 1a-1c) are eliminated, thereby reducing the number of generation/recombination centers therein, thus increasing the lifetime of the depletion capacitor induced below the floating gate.

Fig. 7 depicts the operating voltages on the various electrodes of memory cell 50 during both read and write operations.

Fig. 5 depicts a sample schematic of a four by four memory array utilizing the memory cell embodiment of Figs. 4a-4c. Again, each memory cell 50 includes an access MOSFET device 72 and a floating gate MOSFET device 74. The array is similarly divided into an even number of interlaced blocks (e.g., BLK 1, BLK 2) which need not be physically connected. The access gates (AG) of each word line are, however, all interconnected. A particular block is selected by applying 20 volts to the corresponding programs gates (PG), which are also all interconnected for a given block. The program gate voltage (V_{PG}) of a selected block stays at 20 volts until an entire selected block is accessed during a write cycle. Thus, with a memory array as set forth, cells within an entire block can be "flash" written. Also as shown, adjacent memory cells can share inversion drains (ID) and inversion sources (IS) resulting in a more compact array.

It will be observed from the above description that the present invention contains the features initially set forth herein. In particular, the described memory cell and memory array comprise dense contactless structures having direct write operations such that a conventional block/chip erase operation is unnecessary. Further, the need for a high voltage decode circuit for each word line in a memory array is eliminated, which advantageously enhances memory array density. When in an array structure, blocks of memory cells can be "flash" written, thereby enhancing operational speed. In a preferred embodiment, the invention is implemented in a diffusionless and isolationless design which minimizes generation/recombination centers in the substrate.

Claims

1. A memory cell (10, 50) fabricated on a substrate (12, 52), said memory cell (10, 50) comprising:

   a drain (14, ID);

   an inversion source gate (18, 54) disposed above an upper surface of said substrate (12, 52) such that a depletion source (IS) is induced in said substrate (12, 52) beneath said inversion source gate (18, 54) when a potential is applied thereto, said depletion source (IS) and said drain (14, ID) defining a channel region in said substrate (12, 52);

   an electrically isolated floating gate (26, 62) disposed above the upper surface of said substrate (12, 52), said floating gate (26, 62) partially overlapping said inversion source gate (18, 54) and being electrically isolated therefrom, said floating gate (26, 62) being aligned at least partially over said substrate channel region;

   a program gate (30, 66) disposed above the upper surface of said substrate (12, 52) and being electrically isolated from said substrate (12, 52), said inversion source gate (18, 54) and said floating gate (26, 62), said program gate (30, 66) overlapping at least a portion of said floating gate (26, 62);

   an access gate (34, 70) disposed above the upper surface of said substrate (12, 52), and being electrically isolated therefrom and from said inversion source gate (18, 54), said floating gate (26, 62) and said program gate (30, 66), said access gate (34, 70) being aligned at least partially over said substrate channel region; and

   wherein application of a potential to said inversion source gate (18, 54) and simultaneous application of a potential to said access gat (34, 70) stablishes a cell read cycle to pass charge from said floating gate (26, 62) to said drain (14, IG), and wherein application of ground potential to said inversion source gate (18, 54) and simultaneous application of a potential to said program gate (30, 66) establishes a cell write cycle to selectively charg said floating gate (26, 62) positively or negatively by respectively grounding or applying a potential to said drain (14, ID).

2. The memory cell (10) defined by claim 1, wh rein said drain (14) is disposed within said substrate (12) and is formed by diffusion.

3. The memory c ll (10) defin d by claim 1, wher in said inversion source gate (18) is formed as part of a first layer of polysilicon, said floating gate (26) is formed as part of a second layer of polysilicon, said program gate (30) is formed as part of a third layer of polysilicon, and said access gate (34) is formed as part of a fourth layer of polysilicon.

4. The memory cell (10, 50) defined by claim 1, wherein a single electron injector structure material (28, 64) is disposed between said program gate (30, 66) and said floating gate (26, 62) where said program gate (30, 66) overlaps said floating gate (26, 62), said single electron injector structure material (28, 64) allowing electron flow from said floating gate (26, 62) to said program gate (30, 66).

5. The memory cell (10, 50) defined by claim 1, wherein a single electron injector structure material (24, 60) is disposed between said floating gate (26, 62) and said inversion source gate (18, 54) where said floating gate (26, 62) overlaps said inversion source gate (18, 54), said single electron injector structure material (24, 60) allowing electron flow from said inversion source gate (18, 54) to said floating gate (26, 62).

6. The memory cell (10, 50) defined by claim 1, wherein the capacitive coupling between said program gate (30, 66) and said floating gate (26, 62) is substantially greater than the capacitive coupling between said floating gate (26, 62) and said inversion source gate (18, 54).

7. The memory cell defined by claim 1, wherein the capacitive coupling between said program gate (30, 66) and said floating gate (26, 62) is greater than or equal to the capacitive coupling between said floating gate (26, 62) and the upper surface of said substrate (42, 52).

8. The memory cell (50) defined by claim 1, wherein said drain includes an inversion drain gate (56) disposed above the upper surface of said substrate (52), said inversion drain gate (56) inducing a depletion drain (ID) in said substrate (52) beneath said inversion drain gate (56) when a potential is applied thereto.

9. The memory cell (50) defined by claim 8, further comprising an isolation plate (57) aligned at least partially over said substrate (52) and configured to isolate said cell (50).

10. The memory cell (50) defined by claim 9, wherein said inversion source gate (54) and said inversion drain gate (56) are formed as part of a first layer of polysilicon, said isolation plate (57) is formed as part of a second layer of polysilicon, said floating gate (62) is formed as part of a third layer of polysilicon, said program gate (66) is formed as part of a fourth layer of polysilicon, and said access gate (70) is formed as part of a fifth layer of polysilicon.

11. The memory cell (50) defined by claim 9, wherein said substrate (52) comprises a P-type substrate and said isolation plate (57) is at ground potential.

12. The memory cell (50) defined by claim 9, wherein said floating gate (62) partially overlaps said isolation plate (57), and further comprising SEIS material (60) disposed between said floating gate (62) and said isolation plate (57) where said floating gate (62) overlaps said isolation plate (57), said SEIS material (60) allowing electron flow from said isolation plate (57) to said floating gate (62).

13. The memory cell (50) defined by claim 9, wherein said isolation plate (57) partially overlies each of said inversion drain gate (56) and said inversion source gate (54), and wherein said isolation plate (57) extends between said inversion drain gate (54) and said inversion source gate (56).

14. A memory cell (50) having five layers of polysilicon fabricated on a substrate (52), said memory cell (50) comprising:

a first polysilicon gate layer comprising an inv rsion drain gate (56) and a separat inversion source gate (54), each of said inversion gates (54, 56) being disposed above said substrate (52) such that a

depletion drain (ID) and a depl tion source (IS) ar respectively produced in said substrate (52) beneath said inversion drain gate (56) and said inversion source gat (54) when potentials ar applied th reto, said d pletion sourc (IS) and said depletion drain (ID) d fining a channel region in said substrate (52);

a second polysilicon gate layer comprising an isolation plate (57) for isolating said cell (50), said isolation plate (57) overlying a portion of said substrate (52) and said first polysilicon gate layer (54, 56);

a third polysilicon gate layer comprising an electrically isolated floating gate (62), said third gate layer (62) being isolated from said substrate (52), said first gate layer (54, 56) and said second gate layer (57), said third gate layer (62) overlapping at least a portion of said second gate layer (57) and at least a portion of said substrate channel region;

a fourth polysilicon gate layer comprising a program gate (66), said fourth gate layer (66) being isolated from said substrate (52), said first gate layer (54, 56), said second gate layer (57) and said third gate layer (62), said fourth polysilicon gate layer (66) overlapping at least a portion of said third gate layer (62);

a fifth polysilicon gate layer comprising an access gate (70), said fifth gate layer (70) being isolated from said substrate (52), said first gate layer (54, 56), said second gate layer (57), said third gate layer (62) and said fourth gate layer (66), said fifth polysilicon gate layer (70) being aligned at least partially over said substrate channel region; and

wherein application of a potential to said fourth gate layer (66) and simultaneous grounding of said second gate layer (57) establishes a cell write cycle in which said third gate layer (62) may be selectively charged positive or negative by respectively grounding or applying a potential to said inversion drain gate (56).

15. The memory cell (50) defined by claim 14, wherein said substrate (52) comprises a P-type substrate and said second gate layer (57) is at ground potential.

16. The memory cell (50) defined by claim 14, wherein the capacitive coupling between said fourth gate layer (66) and said third gate layer (62) is substantially greater than the capacitive coupling between said third gate layer (62) and said second gate layer (57).

17. The memory cell (50) defined by claim 14, wherein SEIS material (64) is disposed between said fourth gate layer (66) and said third gate layer (62) where said fourth gate layer (66) overlaps said third gate layer (62), said SEIS material (64) allowing electron flow from said third gate layer (62) to said fourth gate layer (66).

18. The memory cell (50) defined by claim 14, wherein SEIS material (60) is disposed between said third gate layer (62) and said second gate layer (57) where said third gate layer (62) overlaps said second gate layer (57), said SEIS material (60) allowing electron flow from said second gate layer (57) to said third gate layer (62).

19. A memory array fabricated on a substrate, said array comprising:

a plurality of drain lines (D);

a plurality of gate regions, each gate region being disposed above said substrate adjacent one of said plurality of drain lines (D), each of said plurality of gate regions including a floating gate (42, 74);

a plurality of injection source gates, each injection sourc gate being disposed above said substrate (12, 52) adjacent at least one of said plurality of gate regions, each of said plurality of injection source gates inducing a depleted source line in said substrate (12, 52) upon application of a potential thereto, each depleted source line defining a channel region in said substrate (12, 52) extending to an associated one of said plurality of drain lines (D), each of said defined channel regions being at least

partially disposed under the floating gate of the associat d gate region; and

wherein during a read cycl d pl ted sourc lines ar established to pass charge through selected ones of said gate regions to their associated drain lines (D), and during a write cycle depleted source lines are removed to inject charge from selected injection source gates (40, 72) into the floating gates (42, 74) of the associated gate regions.

20. The memory array of claim 19, wherein each of said gate regions and associated drain line (D) and injection source gate comprises a memory cell (10, 50), and wherein each of said plurality of gate regions includes a program gate (40, 72), a plurality of said program gates (40, 72) being electrically connected to form a block of memory cells.

21. The memory array of claim 20, wherein said array is divided into an even number of memory cell (10, 50) blocks and wherein memory cells (10, 50) in two different blocks of said memory array share drain lines (D).

22. The memory array of claim 20, wherein said array is divided into an even number of memory cell (10, 50) blocks and wherein memory cells (10, 50) in two different blocks of said memory array share inversion source gates.

23. The memory array of claim 19, wherein each of said plurality of drain lines (D) includes an inversion drain gate (56) disposed above said substrate (52), each of said inversion drain gates (56) forming a depletion drain (ID) in said substrate with the application of a potential thereto.

24. A memory cell (10, 50) fabricated on a substrate (12, 52), said memory cell (10, 50) comprising:

a drain line (D);

a gate region (42, 74), said gate region being disposed above said substrate (12, 52) adjacent said drain line (D), said gate region including a floating gate (26, 62);

an injection source gate (18, 54), said injection source gate (18, 54) being disposed above the substrate (12, 52) adjacent the gate region, said injection source gate (18, 52) inducing a depleted source line (IS) in said substrate (12, 52) upon application of a potential thereto, said depleted source line (IS) defining a channel region in said substrate extending to said drain line (D), said defined channel region being partially disposed under the floating gate (26, 62) of said gate region; and

wherein during a read cycle a depleted source line (IS) is established to pass charge through said gate region to said drain line (D), and during a write cycle a depleted source line (IS) is removed to inject charge from the injection source gate (18, 54) into the floating gate (26, 62) of the gate region.

25. The memory cell (10, 50) of claim 24, wherein said drain line (D) includes an inversion drain gate (56) disposed above said substrate (52), said drain gate (56) forming a depletion drain (ID) in said substrate (52) with the application of a potential thereto.

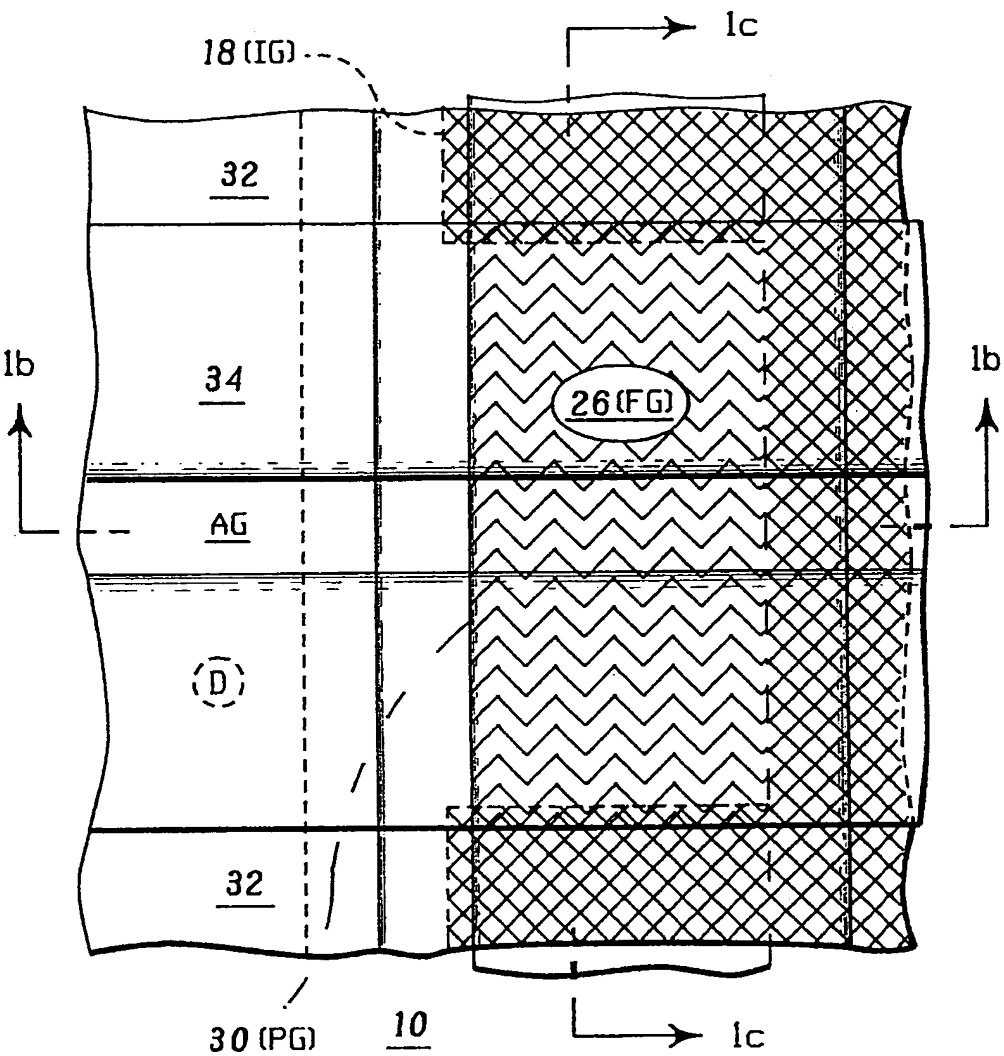

fig. 1a

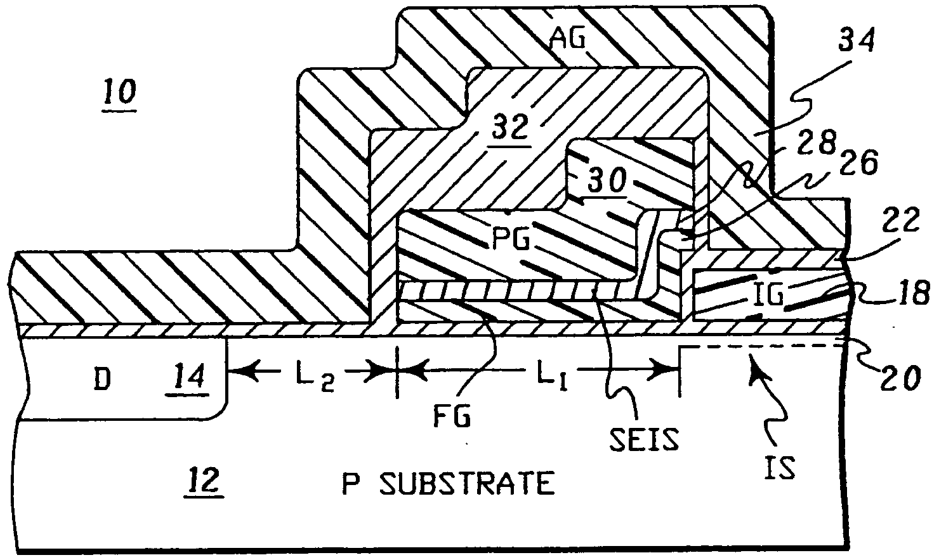
10
AG
34
32
28
26
30
PG
22
IG
18
D
14
L2
L1
20
FG
SEIS
IS
12
P SUBSTRATE

fig. 1b

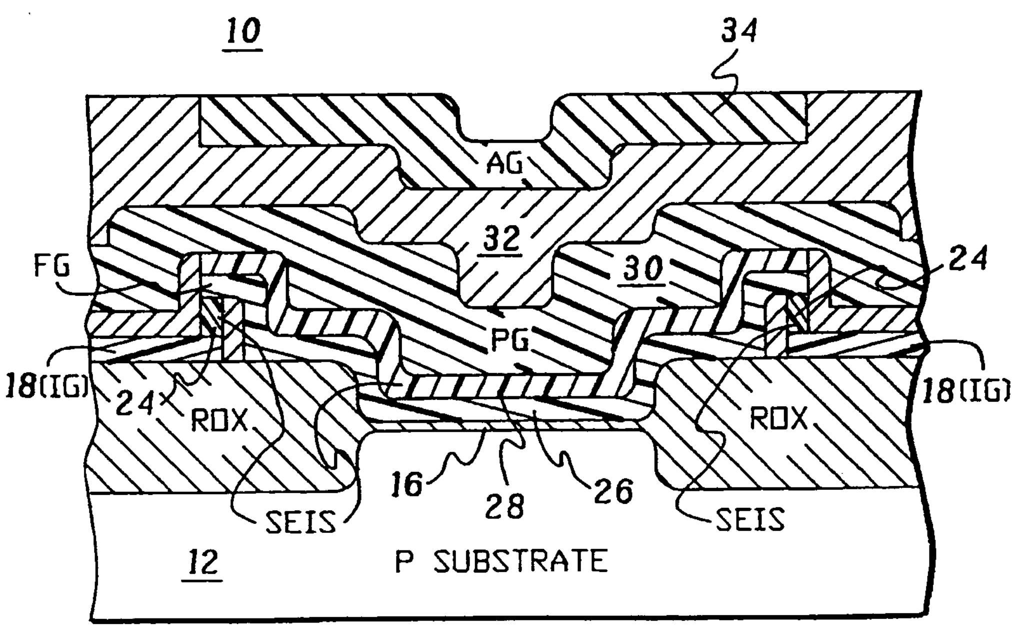
10
34
AG
32
FG
30
24
PG
18(IG)
24
ROX
ROX
18(IG)
16
28
26
SEIS
SEIS
12
P SUBSTRATE

fig. 1c

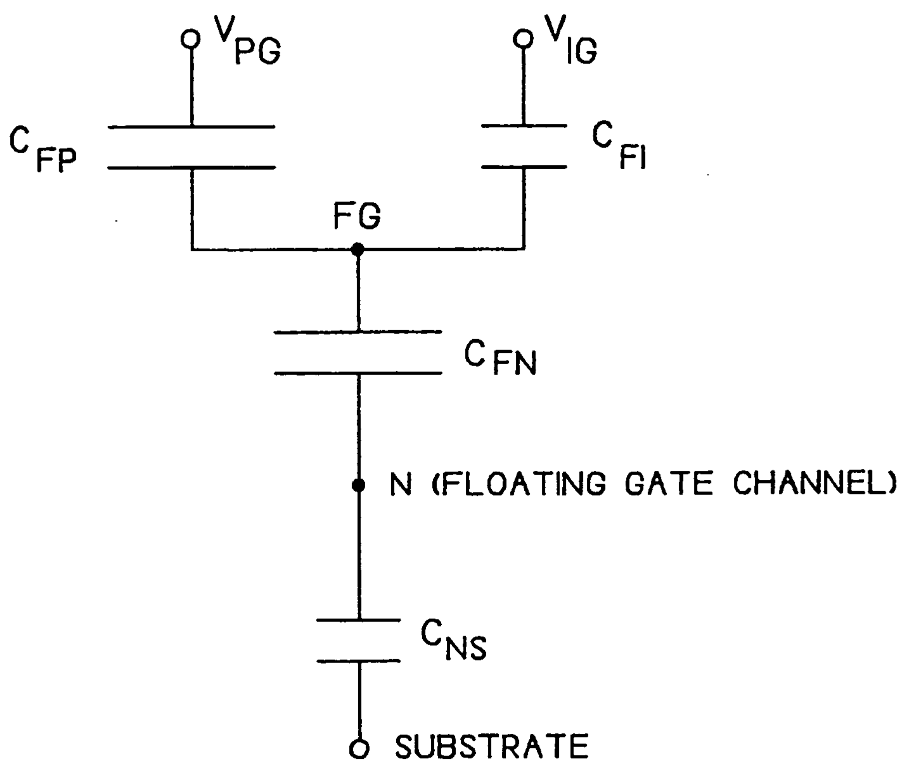

fig. 2

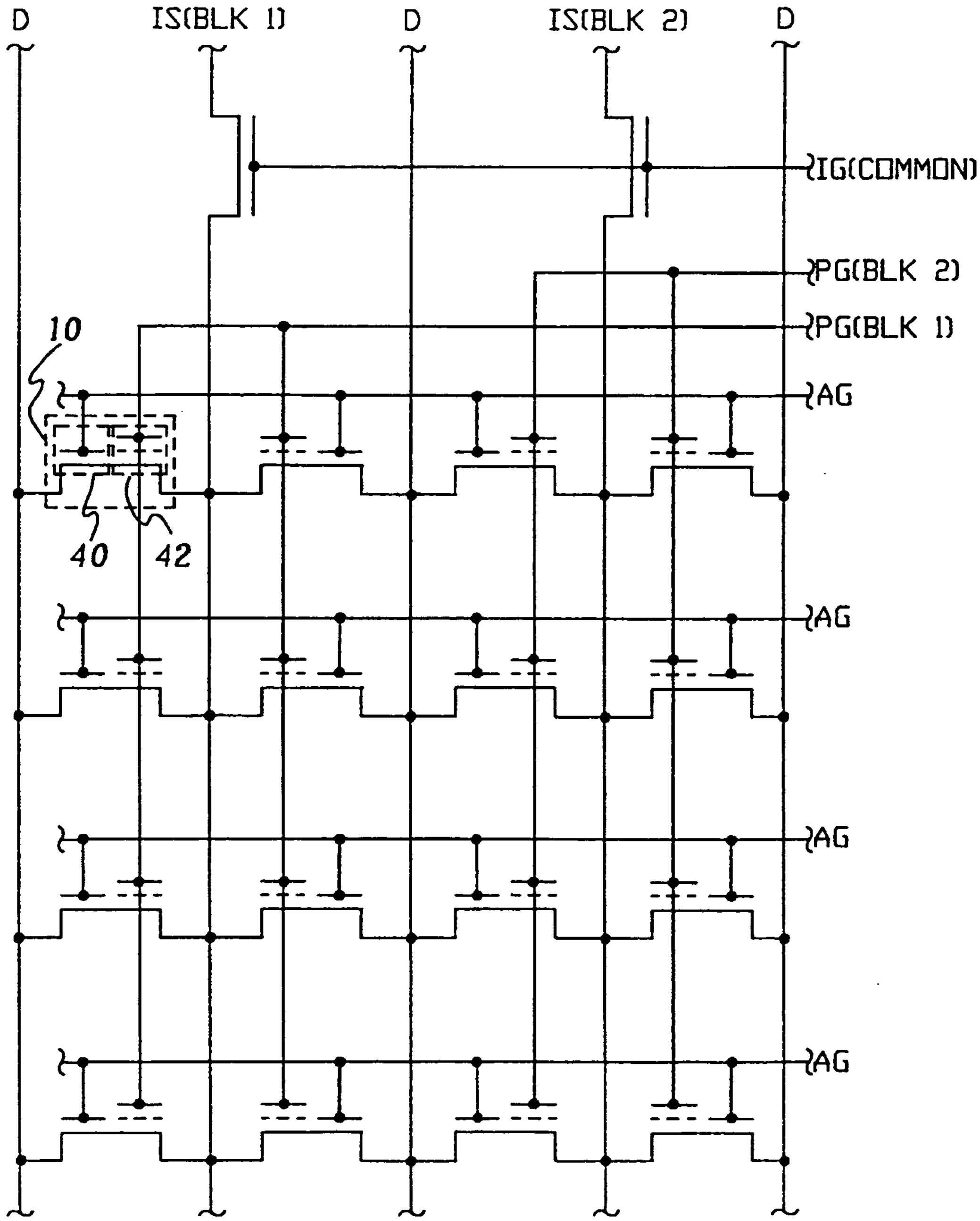

fig. 3

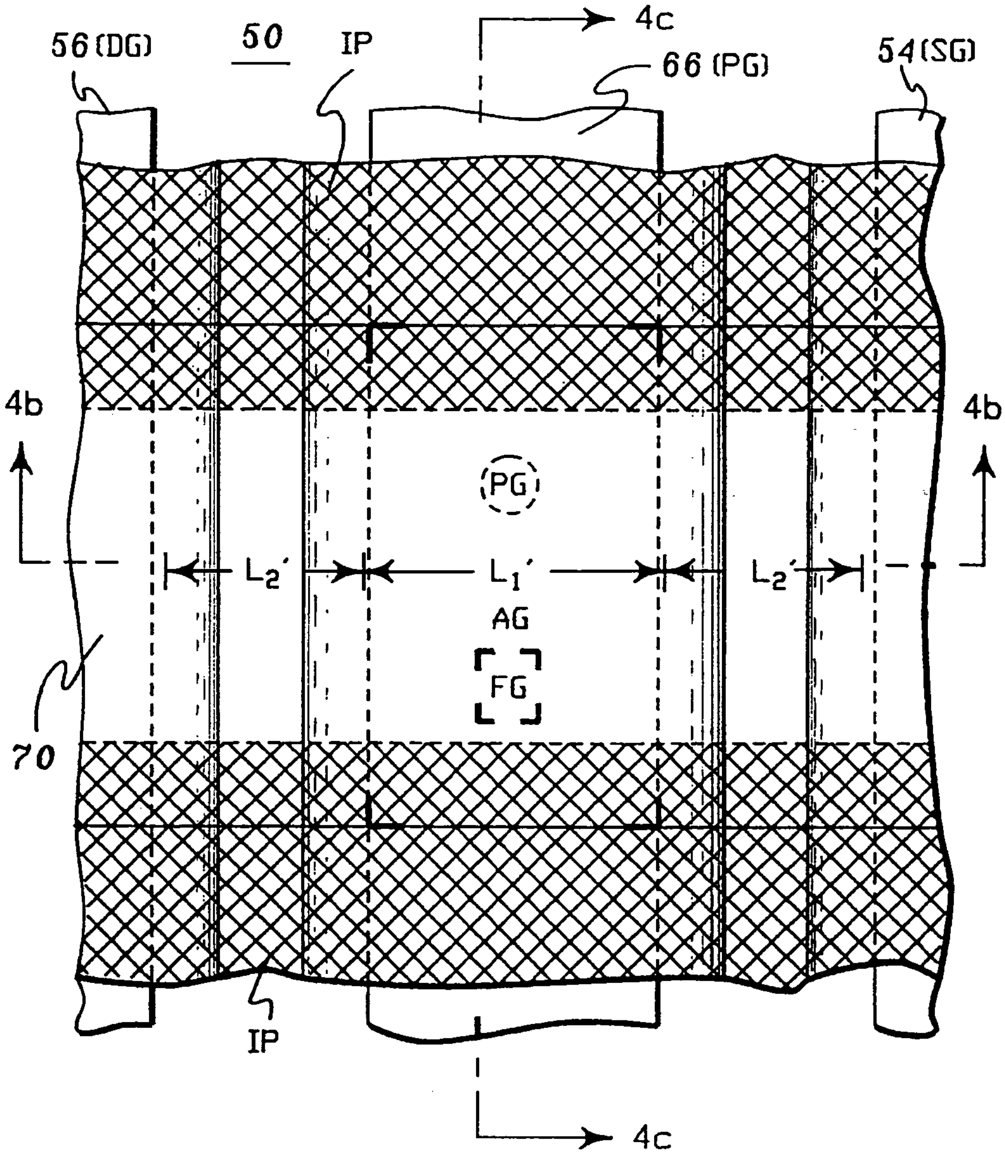

fig. 4a

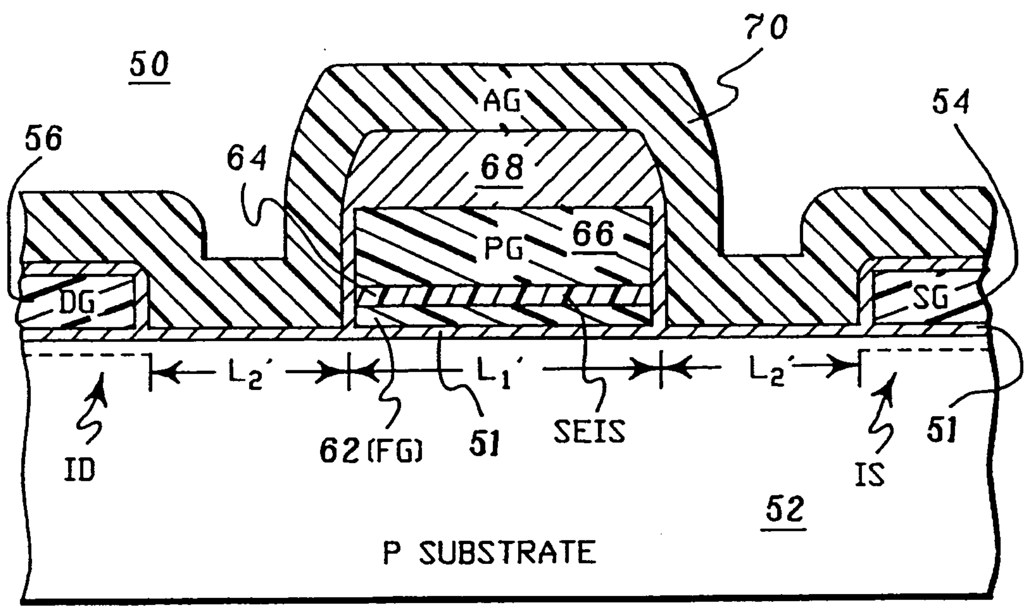
70
50
AG
54
56
64
68
PG
66
DG
SG
L2'
L1'
L2'
62(FG)
51
SEIS
51
ID
IS
52
P SUBSTRATE

fig. 4b

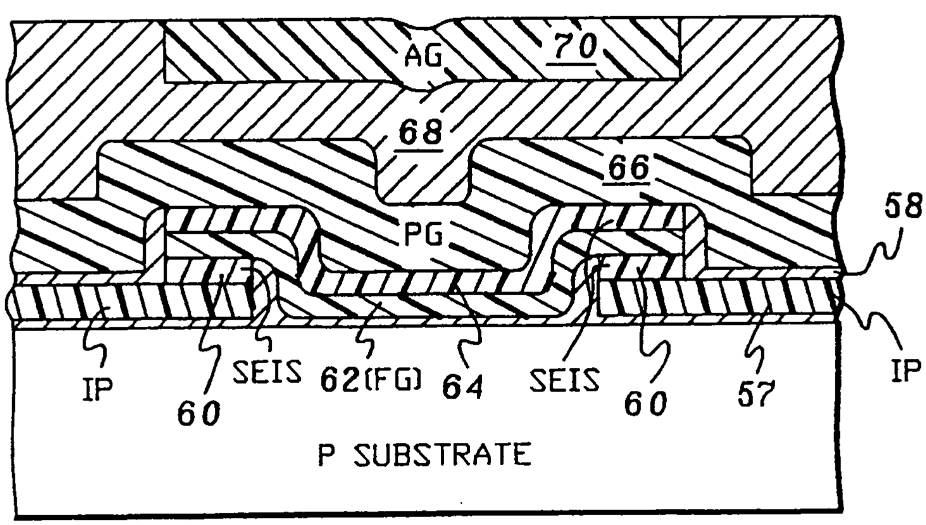
AG
70
68
66
58
PG
IP
60
SEIS
62(FG)
64
SEIS
60
57
IP
P SUBSTRATE

fig. 4c

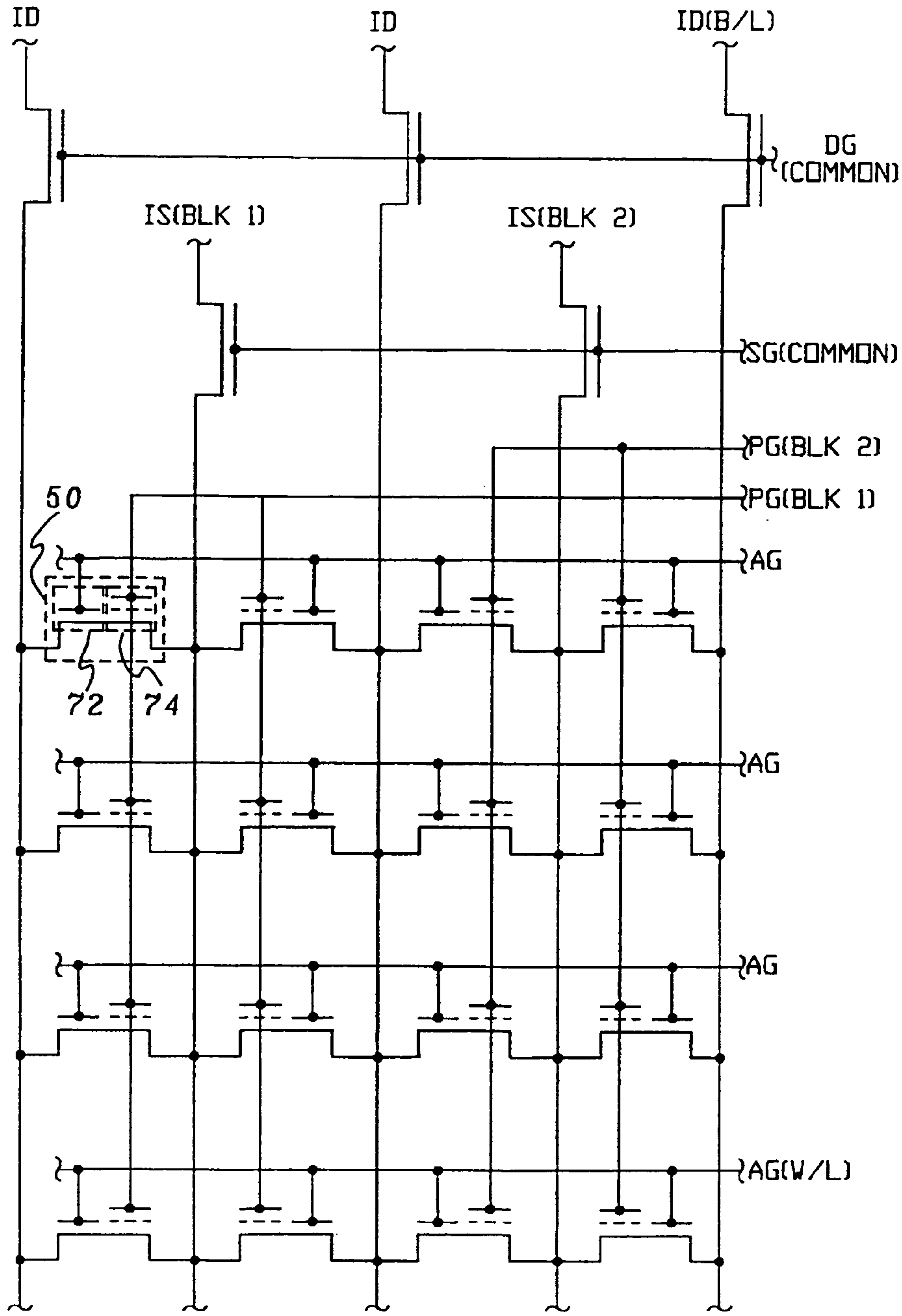
ID
ID
ID(B/L)
DG (COMMON)
IS(BLK 1)
IS(BLK 2)
SG(COMMON)
PG(BLK 2)
PG(BLK 1)
50
AG
72
74
AG
AG
AG(W/L)

fig. 5

	V_{AG}		V_D	V_{IS}		V_{IG}	V_{PG}	
	Sel. Row	Unsel. Rows	All Columns	Sel. Columns	Unsel. Columns	All Columns	Sel. Block	Unsel. Block
READ	3.3V	0V	3.3V	0V	3.3V-V_T	3.3V	0V	0V
WRITE	3.3V	0V	3.3/0V	---	---	0V	20V	0V

fig. 6

	V_{AG}		V_{DG}	V_{ID}	V_{SG}	V_{IS}		V_{PG}		V_{IG}
	Sel. Row	Unsel. Rows	All Cols.	All Cols.	All Cols.	Sel. Blk.	Unsel. Blk.	Sel. Blk.	Unsel. Blk.	All
READ	3.3V	0V	3.3V	$3.3V-V_T$	3.3V	0V	$3.3V-V_T$	0V	0V	0V
WRITE	3.3V	0V	3.3V	Data	0V	---	---	20V	0V	0V

fig. 7